



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,275	03/31/2004	Hung-Ming Chien	58268.00355	5407

32294 7590 10/07/2005

SQUIRE, SANDERS & DEMPSEY L.L.P.
14TH FLOOR
8000 TOWERS CRESCENT
TYSONS CORNER, VA 22182

EXAMINER

MIS, DAVID C

ART UNIT	PAPER NUMBER
----------	--------------

2817

DATE MAILED: 10/07/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/813,275

Applicant(s)

CHIEN, HUNG-MING

Examiner

David Mis

Art Unit

2817

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 12 September 2005.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-32 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 12 September 2005 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

1. OCR (character recognition) reproduction from Applicant's Remarks

section page 11:

"Preliminary Matter

As a preliminary matter, Applicant notes that claim 15, though listed as rejected"

in the summary of the office action, is not actually rejected over any prior art of record.

Applicant notes that claim 15 recites matter that is neither suggested nor disclosed in the cited art. Accordingly, Applicant respectfully requests that claim 15 be considered and allowed."

Applicant has not considered the rejection on page 6 of the Office action in view of Duncan et al. Claim 15 was rejected there.

OCR reproduction from Applicants Remarks section pages 14-16 (Examiner comments inserted as bold type):

"It is respectfully submitted that the cited art of O'Shaugnessy fails to disclose or suggest all the elements of any of the presently pending claims.

O'Shaugnessy is directed to a self-calibrating current mirror and digital to analog converter. O'Shaugnessy, in Figure 3,

describes a current mirror that may serve as a

circuit that reduces the error due to device

mismatch under certain conditions. The

source of input current 318 is

connected to the gates of three transistors (310N312,

320N322A, and 3208/3228).

The transistors are arranged in order to provide a current

mirror that, reduces error due to device mismatch. O'Shaugnessy labels Figure 3, which

contains the above-described circuit, as prior art.

Independent claim 1, upon which claims 2-9 depend, recites "a noise reduction

circuit". **(A circuit that reduces error (eq. 6) in the current mirror output due to process mismatch causes the correct current supply to the oscillator that then operates nominally with respect to this current in linear ranges, and subsequent circuits receive a more nominal oscillator signal – thus allowing less noise. Also, one of ordinary skill in the art would have recognized capacitor 380 as a filter capacitor in accordance with its configuration (which is popular for suppressing noise) and in the absence of any other function attributed to it by O'Shaughnessy")** O'Shaughnessy does not teach or suggest that the described circuit is a noise

reduction circuit. Indeed, O'Shaughnessy does not teach or suggest that any inputs to the circuit will contain noise that can be reduced. Much less does O'Shaughnessy teach or suggest that the noise is bias noise. Accordingly, O'Shaughnessy fails to teach or suggest at least this feature of claim 1 .

The Office Action takes the position that the claimed circuit is known, and that a known circuit cannot be patented by virtue of previously unstated characteristics. The correct test for anticipation, however, is whether each and every element of the claim is found in a single prior art reference. **(Not all LPF means have resistors.)**

Verdegaal Bros. v. Union Oil Co. of Calif., 814 F.2d 628, 631 (Fed. Cir. 1987). Moreover, the appropriate test as to whether an element is taught inherently is whether the missing descriptive matter is necessarily present in the thing described in the reference, and that it would so recognized by persons of ordinary skill. **(The "descriptive matter" is that said in the claims, which is not the same as everything shown in Applicant's drawings, and which is the same as described in the reference. Also, one of ordinary skill in the art was able to recognize the function of capacitor 380.)**

Continental Can Co. USA v. Monsanto Co. 948 F.2d 1264, 1268 (Fed. Cir. 1991).

Additionally, Claim 1 recites "a filter coupled to a gate of a current source for an oscillating circuit to filter a bias noise component into the gate." O'Shaughnessy does not teach or suggest this element.

O'Shaughnessy does not teach that any element of its described circuit serves as a filter, and any structurally similar feature (such as O'Shaughnessy's capacitor 380) is not taught as being appropriately selected to filter noise, as noise is not a described or taught portion of O'Shaughnessy's circuit, as

explained above. **(The "accuracy" function of the resistors taught by O'Shaughnessy (column 5, lines 20-23) reduces the effect of mismatch the same way Applicant uses them to reduce the effect of noise. They necessarily reduce noise by being there. They may also reduce other affect besides process mismatch and noise, but that would not get anyone a patent.)**

Assuming for the moment that O'Shaughnessy provided a filter (not admitted),
O'Shaughnessy's tsIter is not taught as connected to an oscillating circuit. Indeed,
O'Shaughnessy does not

teach or suggest connecting the circuit to any actual output,

(O'Shaughnessy implied the connection of the Fig. 3 circuit to an actual output – 328A and 328B.)

because, as O'Shaughnessy puts it, the Scircuit of FIG. 3 provides improved matching only
over a limited range of current. If the current is too small, the circuit becomes sensitive
to device mismatches.

When current is too large, insufncient supply voltage exists to
drive the output load." Col.

5. 11. 32-37. Thus, although O'Shaughnessy mentions that
current mirrors can be used with balanced modulators, O'Shaughnessy does not suggest
combining the circuit of Figure *3 with a balanced modulator. **(O'Shaughnessy suggests combining the circuit
of Figure 3 with a balanced modulator BY mentioning that current mirrors can be used with balanced
modulators.)** Rather the cited portion

regarding balanced modulators relates to a general description **(The purpose of the general description is to
provide the setting for the specifics that follow.)**, as can be seen at Col. 1,

11. 29-35 (\$tIn general . . ."). Accordingly, O'Shaughnessy fails to teach or suggest at least
these features of claim 1.

Independent claims

10, 19, 24, 28, 31, and 32

each have their own scope, as
explained above.

Claims 10, 19, 24, 28, 31, and 32, however, have some similar recitations to claim 1.

For example, they recite "an oscillating circuit" (Claims 10, 19,

24, 28, 31, and 32) and "a filtering device (in a system for reducing noise)" (Claim 10),

"filtering a bias noise component" (Claim 19), "reducing a bias noise component" (Claim

24), "a noise reduction circuit . . . to reduce a noise component" (Claim 28), "filtering

means for filtering a bias noise component" (Claim 31), and first reducing means for reducing a bias noise component" (Claim 32).

Thus, the same arguments as applied to independent claim 1 may be applied to each of the independent claims."

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10, 12-14, 16-32 are again rejected under 35 U.S.C. 102(b.) as being clearly anticipated by O'Shaughnessy.

O'Shaughnessy disclosed a noise reduction circuit (Fig. 3) comprising a filter (380) coupled to a gate of a current source (310) for an oscillating circuit (Column 1, lines 33-35, where at least the balanced modulators had oscillators, and oscillators were clearly included in this association because they employed current mirrors.) to filter a bias (318) noise component into the gate, and a degeneration circuit (326A, 326B) coupled to a supply for the current source (RVDD), wherein the degradation circuit reduces a gain within the current source (column 5, lines 16-19); ... resistance ... (all circuit elements comprise resistance); ... capacitance ... (380); ... diode ... (column

4, lines 50-51); ... p-channel MOS ... (column 1, line 50 and Figs. 1 and 3); ... low pass filter ... (Fig. 3, 380 is parallel connected to the current mirror node 340); ... filter is coupled to a current mirror ... (Fig. 3, 380 and 340); ... to generate a bias current comprising the bias noise component ... (it inputs and outputs the same signal as Applicants' filter); ... degeneration circuit reduces a supply noise component ... (it inputs and outputs the same signal as Applicants' degeneration circuit); ... noise ... (A known circuit may not be patented by virtue of previously unstated characteristics, and Applicants' circuit does not include materially new features to the known circuit. And it is presumed that the known circuit had the characteristics which Applicant mentions).

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

Art Unit: 2817

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

5. Claims 1-14 and 16-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Shaughnessy in view of Kostelnik et al.

O'Shaughnessy disclosed that said above, but did not say specifically what provided the current at the source of input current (318; Fig. 3). The art is replete with current mirrors, wherever they are employed, having all sorts of stable reference current sources, and for example Kostelnik et al disclosed that band gap bias circuits were known for this purpose; see column 9, lines 1-3. It would have been obvious to one of ordinary skill in the art to have incorporated a band gap circuit in the O'Shaughnessy current mirror to source the input current as disclosed by Kostelnik et al and "motivated" to provide a stable bias for the current mirror as required for stable oscillator operation.

6. Claims 1-10 and 12-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over O'Shaughnessy in view of Duncan et al.

O'Shaughnessy disclosed that said above, but did not show a resistor in the low pass filter. Duncan et al disclosed a noise reduction circuit (Figure 45i, 4524 and 4531) comprising a filter coupled to a gate of a current source for

Art Unit: 2817

an oscillating circuit to filter a bias noise component into a the gate (column 71, lines 11-16). It would have been obvious to one of ordinary skill in the art to have incorporated a resistor in the O'Shaughnessy LPF as disclosed by Duncan et al and "motivated" to provide filter characteristics given by LPF resistors as required by the noise environment.

Rejections based on newly cited art:

7. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for a patent.

Claims 1-4, 6-10, 12-17 and 19-32 are rejected under 35

U.S.C. 102(a.) as being clearly anticipated by Enriquez.

Enriquez disclosed a noise reduction circuit (column 1, lines 12 and 25) comprising a filter (column 2, lines 53-58) coupled to a gate of a current source (Column 3, lines 32-34 where "transistors" are claimed in general.) for an oscillating circuit (Column 1, lines 8-9 "communication systems and components" where oscillators are communications system components that use current mirrors.) to filter a bias noise component into the gate (Column

3, lines 40-46 where the output current depends on the filtered gate voltage.) and a degeneration circuit (Fig. 2, "24" The art being replete with current mirror circuits having emitter/source degeneration means such that they are readily identifiable to one of ordinary skill in the art.) coupled to a supply for the current source (VCC) wherein the degeneration circuit reduces a gain within the current source (degeneration); ... resistance ... (40); ... capacitance ... (42); ... diode ... (11); ... degeneration circuit comprises a resistance ... (24); ... LPF ... (Title); ... supply noise ... (Known function of degeneration means, and necessarily the case.).

8. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

9. The factual inquiries set forth in *Graham v. John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.

4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

10. Claims 1-10 and 12-32 are alternatively rejected under 35 U.S.C. 103(a) as being unpatentable over Enriquez.

Enriquez disclosed that said above where it is construed that when the background specifies the setting for the teachings of the invention as being communication system components, it is suggested that communication system components able to incorporate the invention, and known to one of ordinary skill in the art, like the oscillators, should incorporate the invention, "motivated" to provide the benefits of the invention which were at least as said in column 1, lines 7-27. And it is also construed where the claims in the Enriquez patent are generally to all transistors – PMOS were intended to be covered. It would have been obvious to one of ordinary skill in the art to have applied equivalent circuit transformation to other transistor varieties given the suggestion by Enriquez, and ordinary skill in the art and "motivated" to provide stable oscillator current mirror circuits.

11. Claims 1-32 are rejected under 35 U.S.C. 103(a) as being unpatentable over Enriquez in view of Kostelnik et al.

Enriquez disclosed that said above without specifying in particular communication circuits where the oscillator current mirror has a bandgap reference source. Kostelnik et al, however, did give an example of using a


bandgap reference source. It would have been obvious to one of ordinary skill in the art to have incorporated, as the stable reference source, a bandgap reference source in an oscillator supply circuit "motivated" to have a stable supply (Column 9, lines 1-3.) while using the Enriquez teachings which are provided for the same motivation.

12. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Leonowich disclosed filter capacitor 22 for reducing clock ripple and power supply noise on the current mirror (Column 3, lines 14-23 - where there is no filter resistor and yet it is still a filter capacitor.)

13. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Mis whose telephone number is (571) 272-1765. The examiner can normally be reached on Monday through Thursday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Pascal can be reached on (571) 272-1769. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



David Mis
Primary Examiner
Art Unit 2817